Proposed register mapping, memory-side

Offset	RW	+0 (LSB)	+1	+2	+3 (MSB)
+0	RW	Port A Data			
+1	RW	Port B Data			
+2	RW	Port C Data			
+3	RW	“8255” Control			
+8		I/O Enable Register			
+28	RW	Interrupt Enable Register			
+29	R	Interrupt Status/Clear Bit			
+2C	RW	Debounce Timing Select (LSbit only)			
+2D	RW	Auto Output Mode Enable (LSbit only)			
+30	RW	Interrupt Enables 0-7	IRQ En 8-15	IRQ En 16-23	
+40	RW	Interrupt Status/Clear 0-7	IRQ Stat/Clear 8-15	IRQ Stat/Clear 16-23	
+50	RW	Output GO/DONE status 0-7	Output GO/status 8-15	Output GO/status 16-23	Running, done / not started
+60	RW	Quadrature Control Register (index, IRQen/stat, etc.)			
+64		Quadrature Count value (position, 32-bits)			
+70	RW	Motor Control /Status Bits (go/done,)			
+74	RW	Motor Control Frequency Divisor (20 bits, LSbit justified)			
+78	RW	Motor Control Counts (2’s complement 16 bits)			
+FC	RW	RESET REGISTER			

Per-bit registers @ (bit+1)*100 + 100 (hex)

Bit +00	RW	Bit n Feature Configuration Register (Input)
Bit +04	RW	Bit n Event Configuration/Status Register
Bit +08	RW	Bit n Event / PulseOut Counter 8-bit
Bit +0C	RW	Bit n Event Threshold 8-bit
Bit +10	RW	Pulse Control/Status (direction, forever, done)
Bit +20	RW	Pulse Low duration (as measured, or “inactive” for generation) 16-bits
Bit +24	RW	Pulse High duration (as measured, or “active” for generation) 16-bits
Bit +30	RW	PWM Low-side duration (as measured, or alias for +120 for generation)
Bit +34	RW	PWM High-side duration (as measured, or alias for +120 for generation)
Bit +1C	RW	Frequency Measured (32-bits)

Definition of each register's bits:

Offset	RW	+0 (LSB)
+0	RW	Port A Data
+1	RW	Port B Data
+2	RW	Port C Data
+3	RW	"8255" Control
+8		I/O Enable Register
+28	RW	Interrupt Enable Register
+29	R	Interrupt Status/Clear Bit

As before

Offset	RW	+0 (LSB)
+2C	RW	Debounce Timing Select

This register selects between the default 1µs or 1ms debounce timing constants.

@ +2C	bit	d7	d6	d5	d4	d3	d2	d1	d0
functions		0	0	0	0	0	0	0	1msDebounce

Write "0x01" to the register at +2C to select 1ms debounce, write 0x00 to select the default 1µs timing.

Offset	RW	+0 (LSB)
+2D	RW	Auto Generate Mode

This register selects between the default "manual / simultaneous start" mode and the "Auto start" mode for output pulse (train/pwm) generation.

@ +2D	bit	d7	d6	d5	d4	d3	d2	d1	d0
functions		0	0	0	0	0	0	0	AutoGenerate

Write "0x01" to the register at +2D to select "Auto Generate" mode, write 0x00 to select the default "Manual / Simultaneous" mode. In Auto Generate mode supported outputs will initiate pulse train output generation as soon as the PulseOut Counter register is written (at +bitOfs+10), and PWM outputs will initiate as soon as the PWM Low-side or PWM High-side duration registers are written (at +bitOfs+120/+124 or +130/+134). In Manual / Simultaneous mode pulse (trains/PWM) outputs will not start being generated until the respective GOx bit is set (at either +50, or +bitOfs+10). Therefore in Manual / Simultaneous mode you can preload all the pulse durations and counts, then write to +50 and start the output generation simultaneously on selected bits, while in Auto Generate mode a single byte write to the PulseOut Counter will start the output running.

Offset	RW	+0 (LSB)	+1	+2	+3 (MSB)
+30	RW	Interrupt Enables 0-7	IRQ En 8-15 (reserved/nyi)	IRQ En 16-23	reserved

This register contains the interrupt enable bits, per bit. Bit #0 is the interrupt enable bit for DIO bit #0 (Port A bit 0), etc. Write a "1" to any given bit to enable IRQs on that bit, write "0" to disable IRQs. Reading this register returns last written values.

Offset	RW	+0 (LSB)	+1	+2	+3 (MSB)
+40	RW	Interrupt Status/Clear 0-7	IRQ Status/Clear 8-15 (reserved/nyi)	IRQ Status/Clear 16-23	reserved

Reading these registers returns the interrupt status for each bit. Any bit that reads as "1" indicates the respective bit is trying to generate an IRQ, from among the enabled reasons it might do so. If no interrupt reasons are enabled for any given bit, that bit will always read 0. Writing a 1 to any given bit clears the latched IRQ status. Typically an ISR will read this register, then write back what it read, to clear only those IRQs that occurred before the read and avoid missing IRQs.

Offset	RW	+0 (LSB)	+1	+2	+3 (MSB)
+50	RW	Output GO/DONE status 0-7	Output GO/status 8-15	Output GO/status 16-23	reserved

Writing a "1" to any bit will initiate the configured output signal generation. Writing "1" to multiple bits in one operation allows multiple Pulses, Pulse Trains, or PWM signals to be started simultaneously. Writing a "0" to any given bit has no effect. Reading the register will return a "1" for any bit that has a signal output process currently running, regardless of whether it was started in Manual / Simultaneous mode or by Auto Generate mode. When any given bit's output process ends (the total number of pulses to be output have finished) the respective bit will read as "0".

@ +50	bit	d7	d6	d5	d4	d3	d2	d1	d0
functions		GO7/DONE7	GO6/DONE6	GO5/DONE5	GO4/DONE4	GO3/DONE3	GO2/DONE2	GO1/DONE1	GO0/DONE0
@ +51	bit	d15	d14	d13	d12	d11	d10	d9	d8
functions		GO15/DONE15	GO14/DONE14	GO13/DONE13	GO12/DONE12	GO11/DONE11	GO10/DONE10	GO9/DONE9	GO8/DONE8
@ +52	bit	d23	d22	d21	d20	d19	d18	d17	d16
functions		GO23/DONE23	GO22/DONE22	GO21/DONE21	GO20/DONE20	GO19/DONE19	GO18/DONE18	GO17/DONE17	GO16/DONE16
@ +53	bit	d31	d30	d29	d28	d27	d26	d25	d24
functions		reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Offset	RW	+0 (LSB)
+60	RW	Quadrature Control

The register at +60 configures the Quadrature Counter

@ +60	bit	d7	d6	d5	d4	d3	d2	d1	d0
functions						QuadIndexIRQ/Status	QuadIndexIRQEn	QuadIndexEn	QuadEn

The d0 bit, QuadEn, should be set to 1 to enable quadrature input A/B on Port C0/1, respectively.

Setting the d1 bit, QuadIndexEn, will cause Port C2 to be interpreted as a Quadrature Index pulse; a high input will clear the current Quadrature Count. Clearing the QuadIndexEn bit allows Port C2 to be used for other purposes. While QuadIndexEn is 1 you can enable the Index signal to generate an IRQ by setting QuadIndexIRQEn at d2, and can read the latched IRQ status bit, QuadIndexIRQ/Status, at d3. Writing a "1" to d3 will clear any latched IRQ. The IRQ Status bit is an alias for the Interrupt Status/Clear bit for Port C0 located at bit d0 in +42 (bit d16 in +40 if reading/writing as a 32-bit register).

Offset	RW	+0 (LSB)	+1	+2	+3 (MSB)
+64	RW	Quadrature count bits 0-7	Quadrature count bits 8-15	Quadrature count bits 16-23	Quadrature count bits 24-31

The current Quadrature Count can be read as a 32-bit signed (2's complement) integer from +64. Writing to this register will preload a count value. If QuadIndexEn is "1" a high signal detected at Port C 2 will clear this Quadrature Count value.

Offset	RW	+0 (LSB)
+70	RW	Motor Control

This register controls the Motor Control Output Signal generation feature.

@ +70	bit	d7	d6	d5	d4	d3	d2	d1	d0
functions		0	0	0	0	0	MotorDoneIRQ/Status	MotorDoneIRQEn	GO/DONE

In Manual / Simultaneous mode writing a "1" to the GO bit (d0) will initiate motor signal generation on Port C4/5. Reading the GO/DONE bit will indicate "1" if the motor is still moving. D0 is an alias for the GO20/DONE20 bit at +50. In Auto Generate mode the motor control outputs will begin as soon as the Motor Control Count at +78 is written.

Offset	RW	+0 (LSB)	+1	+2
+74	RW	Motor Control Frequency Divisor (8ns ticks) 20-bit		

Offset	RW	+0 (LSB)	+1
+78	RW	Motor Control Count (16 bits, 2's complement)	

Offset	RW	+0 (LSB)
+FC	RW	RESETs

@ +FC	bit	d7	d6	d5	d4	d3	d2	d1	d0
functions		0	0	0	0	0	Card Reset	Global Counter Reset	Quadrature Counter Reset

Writing a 1 to d1 will reset all event counters. Writing a 1 to d0 will reset the quadrature counter. Writing a 1 to d2 will reset every register as if the board just powered up