ISA ENVIRONMENTAL MONITORING CARD
USERS MANUAL
VPNet Assy No 03-0024

mENVIR-PSM01A.wpd

Chapter 1: Functional Description

GENERAL

The environmental monitor card provides the following basic functions:

The card signal-conditions and monitors two fan speed signals and issues an interrupt if the fan speed goes below a programmed minimum limit. The card also issues an interrupt if the fan speed returns to a level above the minimum speed limit. An error register holds each fan speed limit status and a limit register holds the last counter limit programmed. The same interrupt and error register status operation will occur if the fan cable is disconnected or reconnected.

The card monitors the power supply status bit (**power good**) and issues an interrupt if the power supply status bit changes. An error register holds the status condition. The same interrupt and error register status operation will occur if the power supply cable is disconnected or reconnected. The power supply buzzer can be turned off by software via a card control register bit.

The onboard control register can also be programmed to simulate fan and power supply faults to aid in diagnostics, reset the card and select IRQ level 5, 6 or 7.

FAN SPEED MONITOR

The card measures the speed of two fans using a digital technique of counting the fan's speed signal pulses over a programmed interval**.** Three programmable counters are utilized: Counter 0 is used as a divide-by-N 16-bit counter and is programmed to provide a sample interval for the two fan speed limit counters. Counters 1 and 2 are used as 8-bit countdown counters to indicate when a fan speed drops below a specified speed limit. Both countdown counters must be programmed with the same count limit and the limit is stored in an external card limit register that represents the last limit programmed.

The trigger from counter 0 loads counters 1 and 2 with the programmed limit residing in the counter's internal register and arms the counters. The first pulse received by counter 1 or 2 will set the counter output low and start the countdown of that particular counter. The counter output will remain low while the counter is counting down and will be set high only if the counter completes its countdown before the next trigger from counter 0. Counter 1 and 2 outputs are inverted and latched into the error register bits 7 (**fan 1 fail**) and 6 (**fan 2 fail**) by the next counter 0 trigger, which also reloads the countdown counters and starts the cycle over again.

Each fan speed signal provides two pulses per fan revolution. It is signal-conditioned by a low-pass filter to reduce high frequency noise and glitches and is followed by a Schmitt-trigger gate that provides hysteresis to improve noise immunity and operation with slow signal edges. The fan speed signal is then divided by eight and sent to its countdown counter.

FAN SPEED MONITOR (Continued)

Counter 0

This counter is programmed to run in mode 2 (16-bit rate generator). It provides a divide-by-N counter with an input clock frequency of 873.9 Hz, where N is the count loaded into the counter. The clock comes from the ISA OSC @ 14.31818 MHZ and is divided by a 14-bit counter to 873.912 Hz. The counter output goes low for one clock period (1.14 msec), and after N counts, reloads the initial count and restarts the cycle.

The counter output is used as a strobe to trigger the gates of counters 1 and 2 and to latch the counter outputs and the power supply **power good** status bit into the error register.

The strobe interval is programmable from approximately 2.29 msec to 75 sec (436.7 Hz to 0.0133 Hz).

Counters 1 and 2 Operation Comments

The following sequence of comments illustrates the mode 1 operation of the countdown counters used to monitor fan speed.

1. After the card power-up, the counter is in an indeterminate state. Writing to the counter control word resets the counter control logic and sets the mode 1 counter outputs to a high state. When a limit (count n) is written to a specific counter, the counter's register is loaded.
2. The counter count is loaded from the counter internal register and armed on the rising edge of the counter gate pulse. (counter 0 output trigger)
3. The first clock falling edge after the gate trigger rising edge starts the counter countdown and sets the counter output low. If the fan speed is absence after the gate trigger and never occurs before the next gate trigger, the counter output will remain high and the lack of a fan signal will not be detected. However, the counter trigger and the fan speed signal are exclusive-or'ed together to guarantee that the counter starts the countdown and sets its output low.
4. The down counter decrements at every clock falling edge.
5. The counter output stays low until the count is 0 before the next trigger, at which time it goes high. If the counter does not decrement to 0 before the next counter trigger, the output will remain low indicating fan speed is below the limit.
6. The counter output is latched into the card error register.

POWER SUPPLY MONITOR

The card monitors the power supply status bit, **power good,** and issues an interrupt if the status changes. The **power good** status bit is latched into the error register by counter 0 output trigger. The power supply buzzer is turned on by the supply if the status is bad, but can be turned off via the card control register bit, **buzzer reset**.

INTERRUPTS

An interrupt system generates an edge-activated interrupt for any change in error status of fan 1, fan 2 or power supply. IRQ level 5, 6 or 7 can be selected by software**.**

Chapter 2: Register Description

Address	Read	Write
Base Address + 0		Counter/Timer CTR0
Base Address + 1		Counter/Timer CTR1 and Limit Register
Base Register + 2		Counter/Timer CTR2 and Limit Register
Base Address + 3		Counter/Timer Control Reg.
Base Address + 4	Limit Register	
Base Address + 5	Error Register	
Base Address + 6	Control Register	Control Register

Control Register - R/W

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
swreset	buzzer reset	force fan1 error	force fan2 error	force ps error	intsel1	intsel0	not used

Bit Functional Description:
All single bit fields active high.

All bits set to zero by power up reset or **swreset**.

Bits 1-2 :

(Intsel 1)	(Intsel 0)	Selected
0	0	None
0	1	IRQ5
1	0	IRQ6
1	1	IRQ7

Bit 3: Forces a power supply error.

Bits 4-5: Locks out the fan tachometer input to the fan monitoring circuit.

Bit 6: Turns off the power supply assembly buzzer. The buzzer is turned on and the **power good** status line is forced low by the power supply assembly when a fault is detected by the assembly.

Bit 7: Forces a card reset, which clears all three registers. The reset to the control register is delayed to allow the reset to the other registers to be effective.

Chapter 2: Register Description (Continued)

Limit Register - Write Only

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
L7	L6	L5	L4	L3	L2	L1	L0

Bit Functional Description:

All bits set to zero by power up reset or **swreset**.

L7-L0 form an eight-bit number (from 0 to 255) that relates to the RPM error threshold by the following equation:

Limit = (RPM *2 / 60 / 8 * SEC)

Where SEC is the number of seconds of hysteresis desired (configured in Counter 0).

Error Register - Read Only

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Fan 1 Fail	Fan 2 Fail	PS Fail	X	X	X	X	X

Bit Functional Description:

Unused bits will always read zero.

Bits 7-5 set to zero by power up reset or **swreset.**

Bits are sampled and latched by counter 0 output trigger.

Bit 5: High when the power supply **power good** status line indicates a fault. An interrupt will be initiated each time there is a change in the bit.

Bits 6-7: High when the fan rpm is below the programmed speed limit. An interrupt will be initiated each time there is a change in the bit.

Chapter 3: Address Selection

Addresses 200, 240, 2D0, 300, and 3E0 are all available through A9-A4 jumper selection. Use the following table to determine jumper settings for each of these addresses:

Address	A9	A8	A7	A6	A5	A4
200	OPEN	SHORT	SHORT	SHORT	SHORT	SHORT
240	OPEN	SHORT	SHORT	OPEN	SHORT	SHORT
2D0	OPEN	SHORT	OPEN	OPEN	SHORT	OPEN
300	OPEN	OPEN	SHORT	SHORT	SHORT	SHORT
3E0	OPEN	OPEN	OPEN	OPEN	OPEN	SHORT

Table 3-1: Address Selection Jumpers

Other addresses are possible, using inverse binary representation where SHORT equals Zero and OPEN equals One.

Chapter 4: Programming

See Counter/Timer 82C54 description for details

The card is programmed at the various base addresses described in the previous chapter. For the specific needs of the ENVIR-PSM01, most of the functionality of the 8254 Counter Timer chip can be ignored.

Initialization
This is a breakdown of the algorithm to setup and use the card:
1. Configure Counter 1 for LSB only mode 1.
2. Configure Counter 2 for LSB only mode 1.
3. Configure Counter 0 for LSB+MSB Mode 2.
4. Load the time delay between sequential latch pulses on the error status register.
5. Load the minimum RPM delay that is still considered a valid fan speed.
6. Enable the card to generate IRQs on status changes.

The specifics are shown here:
1. Write 52 hex to Base+3
2. Write 92 hex to Base+3
3. Write 34 hex to Base+3
4. Load CTR0 with the hysteresis strobe divisor (NOTE 1)
5. Load CTR1 and CTR2 with the RPM threshold divisor (NOTE 2)
6. Load the desired IRQ into the control register. (Write 2, 4 or 6 to Base+6)

Note 1: The value of the hysteresis delay is calculated with the following formula:

$$\textbf{Divisor} = \textbf{Frequency}_{\textbf{input}} / \textbf{Frequency}_{\textbf{desired}}$$

Frequency input is 873.9 Hz, so if we want a 0.1Hz update rate (one update each 10 seconds) our equation is 873.9 / 0.1 or 873.9 * 10 = 8739. So we would load 8739 into C0 for a 10 second latch period.

Note 2: The value of the RPM threshold divisor is determined by the following equation:

$$\textbf{Limit} = (\textbf{RPM} * 2 / 60 / 8 / \textbf{Frequency}_{\textbf{desired}})$$

So with a threshold RPM of 3000, the equation simplifies to: $\textbf{12.5} / \textbf{Frequency}_{\textbf{desired}}$. If, as in Note 1, the $\text{Frequency}_{\text{desired}}$ is 0.1 hertz, the Limit Divisor will be 125.

Monitoring
The card will generate IRQs on error conditions as described in the Functional Description chapter. The IRQ selected during initialization can therefore be monitored to determine status conditions on the card. The ISR would be executed on each IRQ, poll the Error Status register at BASE+5 to determine why it was executed, and perform suitable action based on this value. Alternately, the Error Status register may be polled at any time to determine current board status.

Note that the Error Status register updates its contents at the rate of Counter 0's output. Therefore, select a hysteresis load value for counter 0 suitable to your application's needs.

Testing
The card provides a "force error" capability designed to simplify testing the proper functionality of the onboard circuitry. By setting the Force XX Bits in the Control Register at Base + 6, the card will generate the appropriate error condition. Note that the error will occur at the next Counter 0 latch pulse output, based on your initialized hysteresis load divisor. Remember to select an IRQ in this same register access.

For example, to force a Fan 2 error, you would write 12 hex for IRQ 5, 14 for IRQ 6, and 16 for IRQ 7.

Resetting
The card provides a reset capability, should you need it. Setting the most significant bit at Base+6 will reset the hardware to its power-on configuration, including clearing the Reset bit.

Chapter 5: Connector Pin Assignment

Fan Connector Pin	Function
1	Fan 1 Ground
2	Fan 1 +12 VDC Power
3	Fan 1 Speed Input
4	Fan 2 Ground
5	Fan 2 +12 VDC Power
6	Fan 2 Speed Input

Table 5-1: Fan Connector Pins

Power Supply Connector	Function
1	Power Good
2	Ground
3	Buzzer Reset
4	PS +12 Volts

Table 5-2: Power Supply Connector Pins

Chapter 6: Specification

#ISA bus compatible
#Monitors two fan tachometer signals for minimum rpm and cable faults
#Programmable fan rpm limit
#Monitors power supply status and cable faults
#Power supply buzzer turn-off control
#Three software selectable interrupt lines
#Three registers: Control, Limit and Error
#Software reset
#User configurable I/O space addresses
#750 mW maximum board power dissipation
#Fan and Power Supply Connectors
#Card size: 2.5 " high, 4.3 " long