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MODEL 104-AO12-4

USER MANUAL

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Chapter 1: Introduction

The 104-AO12-4 is a multifunction digital-to-analog converter board for use in PC/104-bus computers. In its factory configuration this board has three major functions: 4 Analog Output, 24 Digital Input / Output bits, and a 82C54 Counter timer. However this board can be made to fit an exact application due to its flexibility. There are several factory options available that can be populated or removed. With this board installed a computer can be used as a precision data acquisition and control system or as a signal analysis instrument.

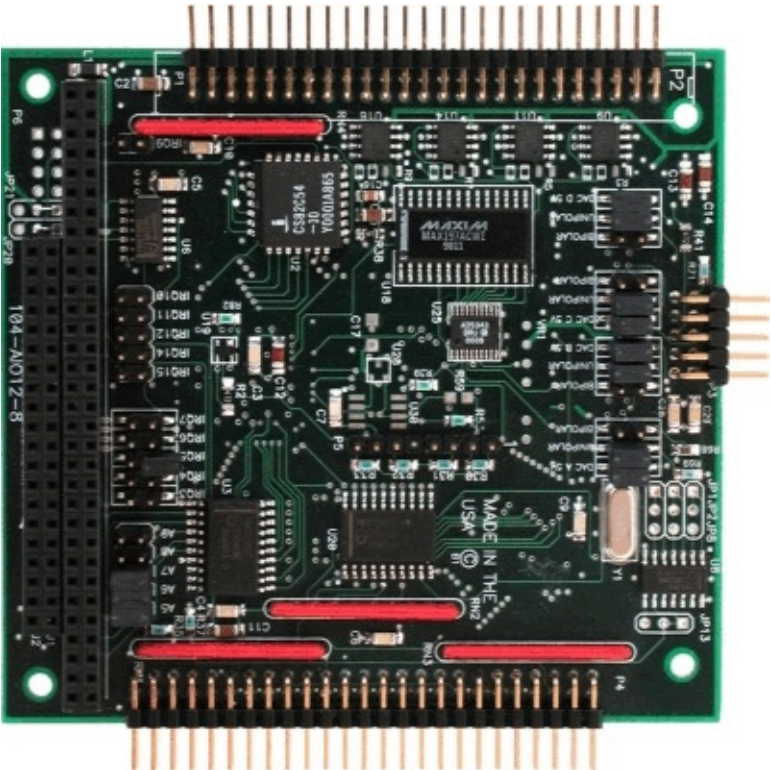


Figure 1-1: Card Photo

Chapter 2: Installation

Before Installing The Card

1. In Windows, install the software from the provided CD. The install program should run automatically; if not, click on the Start Menu, click Run, type `D:\INSTALL`, and click OK or press `Enter`. (If your CD drive is not drive "D", substitute the correct drive letter.) Follow the on-screen prompts to install the software for your card. FileLog.ini will be created in the directory you install to; it contains a list of all files created during the install process.

In DOS, copy the software from the provided CD. The DISKS directory contains packages for various cards; if the package name is not obvious, you can use EDIT to look in the DISKS\DISKS.INI file. Its first section is a list of [card name]=[package] entries. The samples and manual will be in the DISKS\[package] directory. Utilities will be in the DISKS\TOOLS directory.

In Linux, QNX, and other *NIX operating systems, you may find it useful to copy the DOS C samples, which will be in the disks/[package]/DOS/CSAMPLES directory within the CD. The file linux.htm in the root of the CD provides guidelines for converting these samples to Linux, and customers have found these readily useful in other *NIX operating systems.

2. Use Chapter 4, or the Windows setup program, to configure the jumpers on the card.

When selecting an address in DOS, the Findbase utility may be useful. It scans the addresses in the computer to determine which are occupied and suggests an available address. Alternately, if you know a particular address is available (300 (hex) and 100 (hex) are usually available), you can set the card to that address.

If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. After you install the card, if this occurs, power down the stack and try a different address.

To Install the Card

3. Select appropriate standoff hardware for stacking and securing the boards.
4. Power down the PC/104 stack.
5. Install I/O cables onto the card's I/O connectors and secure the stack together using the selected mounting hardware.
6. Power up the PC/104 stack.

After Installing The Card

7. This would be a good time to run one of the sample programs provided on the CD, to test and validate your installation.

Chapter 3: Functional Description

Analog Out

Output ranges of 0-5V, 0-10V, $\pm 5V$ and $\pm 10V$, are field selectable with jumpers. Note that four conversions may take place at once.

Digital I/O

The card has an 82C55A Programmable Peripheral Interface. Ports A and B (16 lines) are buffered, all lines have pull-up resistors to 5V. Port C features Change of State detection.

Counter/Timer

The card has an 82C54 Programmable Interval Timer (3 sixteen bit counter/timers). The user has access to each counter/timer's gate, clock, and output signals. The output of counter one can be used to generate an interrupt. The software package supports counting events, frequency output, pulse and frequency measurement.

Flexibility

Interrupts from each function can eliminate the need for polling. Interrupts are individually enabled or disabled via software. A status register is provided to determine the interrupt source.

These functions are available in many configurations. This gives the user the ability to specify exactly what's needed to minimize costs. Your board can be populated with any combination such as Digital I/O with 4 DAC channels, or 2 DAC channels with 82C54 Counter/Timers. This is indicated by a label on the PC/104 connector that has a part number ending in -S0X, where X indicates a unique number identifying a special configuration.

The following are also available as factory options:

A $\pm 12V$ DC/DC converter is available as a factory option. While $\pm 12V$ is part of the PC/104 bus spec, the bus is often implemented without these voltages available. This DC/DC converter allows the card's analog functions to operate on such a bus.

The standard card has most of the functionality that the card is capable of with the exception of the $\pm 12V$ DC/DC converter and programmed digital I/O.

Chapter 4: Option Selection

The card has jumpers to select the following options:

- Base address
- IRQ level
- DAC output voltage ranges
- 8255 Mode 1 Inversion of Digital I/O
- +/-12V Power Options

Base Address

The base I/O address is set by these jumpers, next to the PC/104 connector. The jumper posts are marked A5 through A9; A5 is the least significant bit of the address. The base address can be selected anywhere below 400 hex, provided that the card does not overlap any other device in the system. In DOS, the Findbase utility can help you select an available block of addresses. The card occupies 32 (20 hex) addresses, from Base (the base address) to Base + 1F hex.

Addresses below 100 (hex) are occupied on most desktop computers; however, embedded systems may have available addresses in this range.

In order to configure the desired address, the hexadecimal address must be converted to a binary representation. For example, as illustrated below, jumper selection corresponds to hex **2C0** (or binary **10 101x xxxx**). The "x xxxx" represents address lines A4 through A0 used on the card to select individual registers as described in the Chapter 5, Programming of the manual.

Hex Representation	2		C		
Conversion Factors	2	1	8	4	2
Binary Representation	1	0	1	1	0
Jumper Setting	Out	In	Out	Out	In
Jumper Label	A9	A8	A7	A6	A5

Table 4-1: Example Address Selection

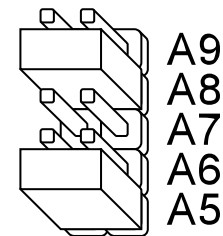


Figure 4-1: Example Address Jumpers

Please note that "1" = "Out"(no jumper) and "0" = "In"(jumper installed).

Review the Address Selection Table carefully before selecting the card address. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. If you have doubts concerning available addresses in your particular computer, use the FINDBASE utility provided to determine available addresses.

The following table provides a convenient reference for all address jumper configurations. IN indicates the jumper is installed.

A9	A8	A7	A6	A5	Address Range
					3E0h - 3FFh
				IN	3C0h - 3DFh
			IN		3A0h - 3BFh
			IN	IN	380h - 39Fh
		IN			360h - 37Fh
		IN		IN	340h - 35Fh
		IN	IN		320h - 33Fh
		IN	IN	IN	300h - 31Fh
	IN				2E0h - 2FFh
	IN			IN	2C0h - 2DFh
	IN		IN		2A0h - 2BFh
	IN		IN	iN	280h - 29Fh
	IN	IN			260h - 27Fh
	IN	IN		IN	240h - 25Fh
	IN	IN	IN		220h - 23Fh
	IN	IN	IN	IN	200h - 21Fh
IN					1E0h - 1FFh
IN				IN	1C0h - 1DFh
IN			IN		1A0h - 1BFh
IN			IN	IN	180h - 19Fh
IN		IN			160h - 17Fh
IN		IN		IN	140h - 15Fh
IN		IN	IN		120h - 13Fh
IN		IN	IN	IN	100h - 11Fh

Table 4-2: Converting Base Addresses To Jumper Settings

IRQ

If you will be using the IRQ features of the card, install one of the IRQ jumpers next to the PC/104 connector. If you are not using these features, simply do not install any IRQ jumpers.

DAC Ranges

Each DAC has a block of three jumpers, 5V, UNIPOLAR, and BIPOLAR. These blocks are in a row far from the PC/104 connector, labeled DAC A, DAC B, DAC C, and DAC D. Install jumpers for each DAC depending on the range desired for it, as shown on the following table. IN means to install the specified jumper.

Range	Jumpers		
	5V	UNIPOLAR	BIPOLAR
±5V	IN		IN
0-5V	IN	IN	
±10V			IN
0-10V		IN	

Table 4-2: DAC Range Selection

8255 Mode 1 Inversion

For normal use of the digital I/O bits, install these jumpers in their Noninverted positions, as shown on the Option Selection Map below. If you're using the digital I/O for 8255 Mode 1 communication with another 8255, certain bits on Port C will need to be inverted. These jumpers invert the bits for you. They're located far from the PC/104 connector, below the DAC range jumpers, labeled JP1, JP2, JP8, and JP13, as shown on the Option Selection Map below.

Inverting bits 1 and 2 allows Port A to communicate with a noninverted Mode 1 port. Install JP1 (bit 1) and JP2 (bit 2) in the Inverted positions for this. Inverting bits 5 and 6 allows Port B to do the same. Install JP8 (bit 5) and JP13 (bit 6) in the Inverted positions for this.

The inverters treat bits 1 and 5 as outputs and bits 2 and 6 as inputs, which is how they're used in 8255 Mode 1. When noninverted, these bits can freely be inputs or outputs.

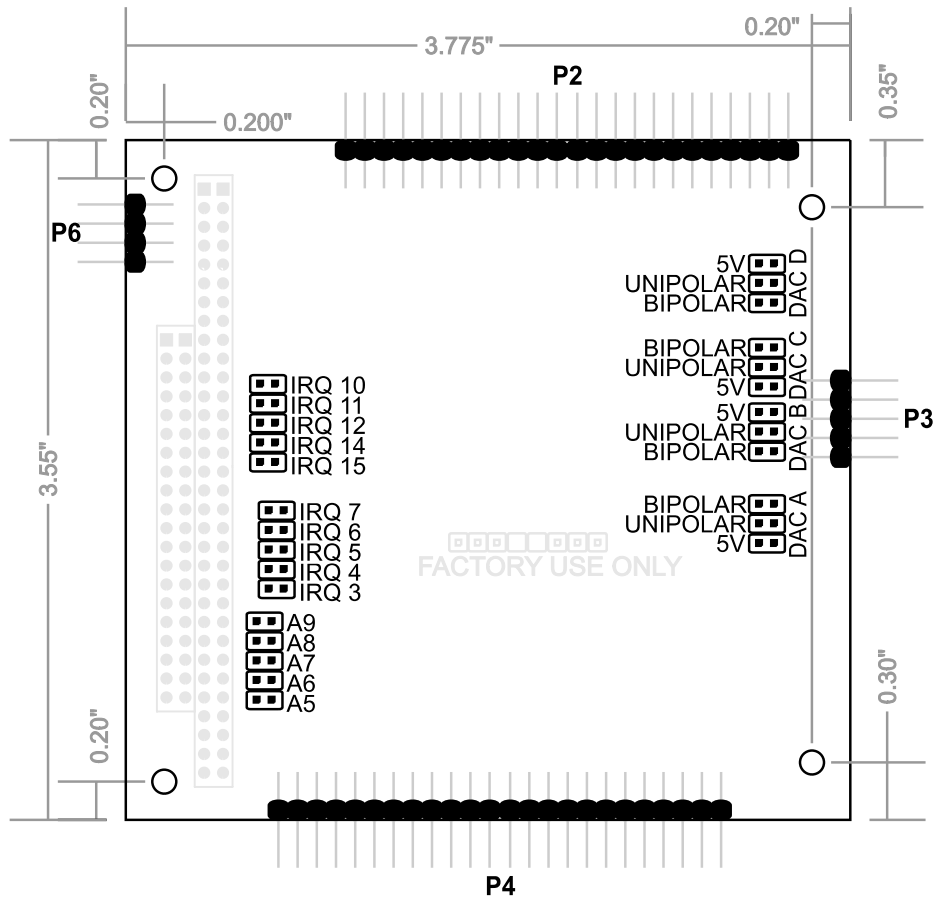


Figure 4-2: 104-AO12-4 Option Selection Map

Chapter 5: Programming

The card uses 24 consecutive registers in I/O space as follows:

Offset	Read Function	Write Function
00h	Card Status / Clear Card Status	IRQ Clear
01h	Interrupt Status	Interrupt Enables
02h		
03h		
04h		D/AC 1 LSB
05h		D/AC 1 MSB
06h		D/AC 2 LSB
07h		D/AC 2 MSB
08h		D/AC 3 LSB
09h		D/AC 3 MSB
0Ah		D/AC 4 LSB
0Bh		D/AC 4 MSB
0Ch	Counter/Timer 0 Value	Counter/Timer 0 Load Value
0Dh	Counter/Timer 1 Value	Counter/Timer 1 Load Value
0Eh	Counter/Timer 2 Value	Counter/Timer 2 Load Value
0Fh		Counter Control
10h	Digital I/O Port A	Digital I/O Port A Output Value
11h	Digital I/O Port B	Digital I/O Port B Output Value
12h	Digital I/O Port C	Digital I/O Port C Output Value
13h	Digital I/O Status (Modes 1 & 2)	Digital I/O Command Byte
14h		Digital I/O Buffer Control
15h		
16h		Timer Triggered Conversion Enables
17h	COS Status / Clear COS Status	

Table 5-1: Register Map

Base + 0: Card Status

operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
READ	reserved	Change of State	reserved	reserved	reserved	IRQ Enabled	reserved	reserved

This register shows the state of the COS event and the global interrupt enable. The interrupt enables/disables have no effect on the events shown in this register. All bits are active HIGH. Also, the event bit is latched; when an event occurs, its bit goes HIGH until this register is read. Reading this register clears it.

Writing to this register clears IRQs (see the description of IRQ enables).

Bit 6 goes HIGH when any DIO bit on Port C changes.

Bit 2 reflects the global interrupt enable written to Base + 1. This is not an event, and is not cleared when read.

Base + 1: Interrupt Enables, Interrupt Status

operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
READ	always zero	Change of State IRQ	Counter 1 IRQ	Digital I/O Port C3 IRQ	Digital I/O Port C0 IRQ	IRQ Event	always zero	always zero
WRITE		Change of State IRQ Enable	Counter 1 IRQ Enable	Digital I/O Port C3 IRQ Enable	Digital I/O Port C0 IRQ Enable	Global IRQ Enable		

All bits are active HIGH. Reading this address accesses the Status register. Writing to this address affects the Enables register. Note that the register that's written to is not the same register that's read at this address.

Interrupts from this card can be shared. The IRQ driver will pull the PC/104 interrupt line LOW for 500nS, briefly drive it HIGH, and then tri-state. After an interrupt is generated another won't be allowed until the IRQ has been cleared (write to Base+0) and the data read (for some event types).

If multiple enabled events occur (for example, a Counter 1 timeout and a Port C change of state), and only one is cleared (for example, by writing to Base+0 but not reading the COS data), the other event will cause another interrupt.

Set bit 2 HIGH to enable interrupts from the card. The default after system RESET is LOW. Without this global enable set, the card will not generate interrupts of any kind. If an interrupt has been generated by the card, this bit will be HIGH when read.

Set bit 6 HIGH to enable interrupts from the Change of State detection circuit at DIO Port C. When read, bit 6 is HIGH if a change of state generated an interrupt that was not yet cleared. Read Base+17 to get the COS data, and write to Base+0 to clear the card's interrupt so it can generate another.

Set bit 5 HIGH to enable interrupts from falling edges of Counter 1. When read, bit 5 is HIGH if the counter generated an interrupt that was not yet cleared. Write to Base+0 to clear the card's interrupt so it can generate another.

Set bits 4 and 3 HIGH to enable interrupts from rising edges of DIO Port C bits 3 and 0, respectively. When read, bits 4 and 3 are HIGH if these bits generated an interrupt that was not yet cleared. Write to Base+0 to clear the card's interrupt so it can generate another.

Using The Digital To Analog Converters

A conversion begins after the most significant byte (of which only the lower 4 bits will be used) has been written to a DAC. The input coding to the DACs are offset binary. Discounting offset and gain errors, the output voltage is given by

$$V_{out} = (\text{Span} * \text{Counts} / 4096) + \text{Offset}$$

where Counts = the code written to the DAC (a number between 0 and 4095 decimal).

Range	0-5V	0-10V	±5V	±10V
Span	5	10	10	20
Offset	0V	0V	-5V	-10V

On power-up, the output values will be at the most negative for the selected range.

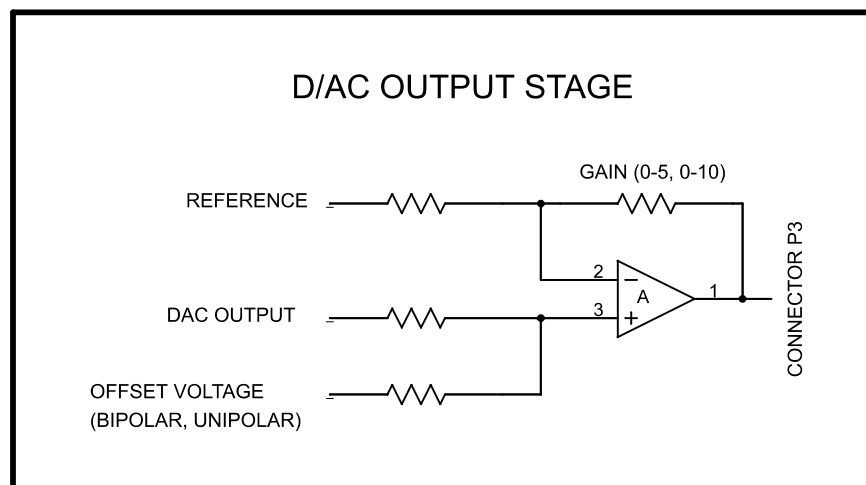


Figure 5-2: DAC Output Stage

Using Counter 1 To Trigger A/D And D/A Conversions

In Mode 2 the Counter/Timer chip will generate a 1 microsecond negative going pulse at a programmed rate. If bit 0 of the Timer-Triggered Conversion Enables register (base address + 16h) is set high, the DAC chip will initiate conversions on the tick.

All of the DACs present will be updated simultaneously. Typically, the user would configure the board to generate an interrupt on the tick from counter 1 and also enable DAC conversions triggered by the same tick.

Using The Digital Input/Output Ports

This function is based on an 82C55A chip. Please refer to file 8255.pdf in the \CHIPDOCS directory on the CD.

On power-up or on Reset the circuit will be in the mode 0 input state. That is, ports A and B (each 8 bits) and ports C 'upper' and C 'lower' (each 4 bits) will be readable, and any floating pins at connector P4 will be high.

Base + 13: Digital I/O Command Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Set Flag	Group A Mode	Group A Mode	Port A Direction	Port C Upper Direction	Group B Mode	Port B Direction	Port C Direction
1 = Active	1 = Mode 2 0 = use Bit 5	1 = Mode 1 0 = Mode 0	1 = Input 0 = Output	1 = Input 0 = Output	1 = Mode 1 0 = Mode 0	1 = Input 0 = Output	1 = Input 0 = Output

To change Port A and Port B I/O configuration, there are two modes. In the default mode the buffers' direction is automatically set by the command-byte. This mode is designed to support 'off the shelf' software.

If bit 0 of the Digital I/O Buffer Control register is set (base address + 14h), an alternate mode is entered (all other bits don't care). When software configures a port to be an output the lines will be low (quirk of the chip). Since most control signals are active-low, on this event the card will tri-state the associated buffer and allow the lines to be pulled high. Software would then initialize the port's output and re-enable the buffer(s).

The circuit contains a latch that controls the data-directions and output-enables of the 8 bit buffers on ports A and B (Port C is not buffered). This latch has the same address as the 8255 command byte but can only be written to if the chip is in mode 0 and if Bit 7 is low. To automatically set the data-direction for each port software must simply write the control byte a 2nd time but with Bit 7 cleared.

This circuit can, as a factory installed option, operate in 8255 programmed I/O Modes 1 and 2. Note that if Bit 6 is set then Bit 5 is unused.

Change-Of-State (COS)

If any bit of Port C changes state, this event is noted in the card status register(Base+0), an interrupt is generated if enabled(at Base+1), and the specific bit that changed is noted in the COS status register(Base+17). Multiple changes are accumulated in the COS status register until read.

For example, if Port C changed from "50" to "40", bit 4 has changed, so the COS status register will contain the value "10" (bit 4 high). If Port C then changed to "60", bit 5 has changed, so the COS status register will contain the value "30" (bits 4 and 5 high). If it's then read, this "30" will be read, and it will be cleared to "00".

Using The Counter/Timer Circuit

This function is based on an 82C55A chip. Please refer to file 8255.pdf in the \CHIPDOCS directory on the CD.

We suggest using mode 2, rate generator, for timer ticks and for timer triggered events. Note that the outputs of the counters go high when each counter's command is written to the Counter/Timer chip. Please see the 82C54 datasheet in the \ChipDocs directory.

Base + F: Counter Control Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WRITE	Counter Selection bit 1	Counter Selection bit 0	Read/W rite Selection bit 1	Read/W rite Selection bit 0	Mode Selection bit 2	Mode Selection bit 1	Mode Selection bit 0	Binary Coded Decimal

For bits 7 and 6:

00 = select counter 0, 01= select counter 1,
10 = select counter 2, 11 = read back

For bits 5 and 4:

00 = counter latch, 01= read/write LSB, 10 =
read/write MSB, 11 = read/write LSB MSB

For bits 3, 2, and 1:

000 = mode 0, 001 = mode 1, 10 = mode 2,
11 = mode 3, 100 = mode 4, 101 = mode 5

For bit 0:

0 = 16 bit binary, 1 = binary coded decimal

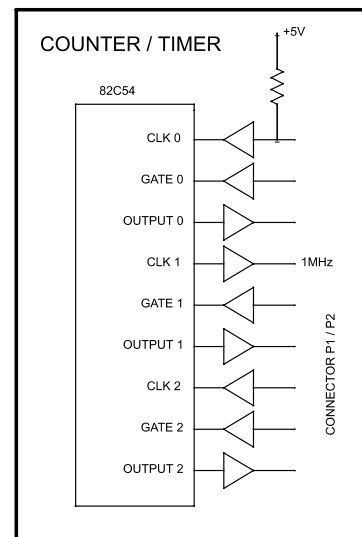


Figure 5-3: Counter/Timer Interface

Chapter 6: Connector Pin Assignments

P3, DAC

Pin 1 Ground	Pin 2 DAC A Output
Pin 3 Ground	Pin 4 DAC B Output
Pin 5 Ground	4.096V Reference Output
Pin 7 Ground	Pin 8 DAC C Output
Pin 9 Ground	Pin 10 DAC D Output

Each DAC output can drive up to $\pm 10\text{mA}$. Due to a limitation of the power supply, the total drive of these four signals should be kept below 20mA. If $\pm 12\text{V}$ power is supplied at the ISA bus connectors or at P6, there isn't a cumulative drive current limit.

Each DAC output has three configuration jumpers. If the jumper labeled 'DAC x 5V' (where x is either A, B, C, or D) is in place, the range is limited to 5V (0-5V or $\pm 5\text{V}$). If the jumper labeled 'UNIPOLAR' is in place the range is limited to 0-5V or 0-10V. If the jumper labeled 'BIPOLAR' is in place the range is either $\pm 5\text{V}$ or $\pm 10\text{V}$. Note that 'UNIPOLAR' and 'BIPOLAR' are mutually exclusive.

P1, Timer/Counter (see description)

Pin 1 Ground	Pin 2 Clock 0 Input
Pin 3 Gate 0 Input	Pin 4 Out 0 Output
Pin 5 1MHz Output	Pin 6 Gate 1 Input
Pin 7 Out 1 Output	Pin 8 Clock 2 Input
Pin 9 Gate 2 Input	Pin 10 Out 2 Output

Pins 2 and 8 are the clock or event inputs for the Programmable Interval Timer counters Zero and Two and are pulled-up to +5V through a 10K resistor. 8MHz is the maximum frequency. Pin 5 is an output of the 1MHz square wave applied to the clock input of counter one.

Pins 3, 6, and 9 are the gate inputs and are pulled-up to +5V through a 10K resistor. Pull these inputs low to pause/disable the counters.

Pins 4, 7, and 10 are the counter outputs and can not tri-state.

Either TTL or CMOS signal levels are acceptable at all inputs. The 1MHz clock signal (pin 5) is a CMOS output.

P4, Digital I/O

Pin	Signal	Pin	Signal
50	Ground	49	+5V FUSED
48	Ground	47	Port A Bit 0
46	Ground	45	Port A Bit 1
44	Ground	43	Port A Bit 2
42	Ground	41	Port A Bit 3
40	Ground	39	Port A Bit 4
38	Ground	37	Port A Bit 5
36	Ground	35	Port A Bit 6
34	Ground	33	Port A Bit 7
32	Ground	31	Port B Bit 0
30	Ground	29	Port B Bit 1
28	Ground	27	Port B Bit 2
26	Ground	25	Port B Bit 3
24	Ground	23	Port B Bit 4
22	Ground	21	Port B Bit 5
20	Ground	19	Port B Bit 6
18	Ground	17	Port B Bit 7
16	Ground	15	Port C Bit 0
14	Ground	13	Port C Bit 1
12	Ground	11	Port C Bit 2
10	Ground	9	Port C Bit 3
8	Ground	7	Port C Bit 4
6	Ground	5	Port C Bit 5
4	Ground	3	Port C Bit 6
2	Ground	1	Port C Bit 7

The digital I/O bits are arranged in an industry standard configuration.

Pin 1 can be identified by the square pad on the bottom of the board. Also, with the PC/104 connector closest to you, pin 1 of P4 is on the bottom row, closest to you.

P6, $\pm 12V$ Power

Pin	Signal	Pin	Signal
1	Ground	2	N/C
3	Ground	4	+12V
5	Ground	6	-12V
7	Ground	8	N/C

Normally, the card takes $\pm 12V$ power from the PC/104 bus. However, it can be used on a PC/104 stack that does not provide $\pm 12V$ power by providing it here on P6.

Note:

Pins 4 and 6 of P6 are connected to the corresponding lines of the PC/104 bus. If your PC/104 stack provides $\pm 12V$ power, it will be sourced on these pins.

Appendix A: Technical Specifications

Analog Outputs

Feature	Value	Feature	Value
Channels	4	Voltage Ranges	0-5V, 0-10V, $\pm 5V$, $\pm 10V$
Conversion Frequency	100K Conversions per second	Resolution	12-Bit
Output Drive Capability	$\pm 10mA$ per channel	Power-Down Mode Current Draw	1 μA , maximum
Relative Accuracy	± 0.2 LSB, typical	Trigger Source(s)	Software selectable for program command or programmable timer

Digital Input/Output

Feature	Value	Feature	Value
Programmable Peripheral Interface	82C55A	Channels	24, pulled up to 5V via 10K (or pulled down to ground)
Buffered Channels	16 (ports A & B)	Sink & Source Current	64mA & 32mA
Modes supported	mode 0 (1 and 2 are factory options)	Change of State Detection	8 inputs (port C)

Counter/Timer

Feature	Value	Feature	Value
Peripheral Interface Timer	Type 82C54	Counters	3 x 16-Bit down counters
Clock Frequency Output	1 MHz	Inputs/Outputs	Fully Buffered
Native Modes	Pulse on terminal count, retriggerable one-shot, rate generator, square wave generator, software triggered strobe, hardware triggered strobe		
Software support	Event counter, frequency output, frequency and pulse measurement		

General

Feature	Value	Feature	Value
Power Required:	+5V @ 40mA, $\pm 12V$ @ 30mA +5V @ 240mA w/optional $\pm 12V$ DC/DC conv.	Environmental	0 to +70°C standard, w/o DC/DC converter -40 to +85°C
Interrupt Requests:	Eleven channels, IRQ 3-7, 9-12, 14, 15	Interrupt Status Register Interrupt Enable/Disable	Indicates source(s) of interrupt Software Controlled

Appendix B: Debug Scripts

In DOS, on the command line type “debug < adc_0.dbg” or “debug < counter_0.dbg” or “debug < filename.dbg”. These scripts assume that the board’s address is 0300h.

This script will use DAC A to output a stepped voltage test pattern. Connect pin 2 of connector P3 to pin 4 of connector P2 if the instrumentation amplifier is present or to pin 6 if the amplifier isn’t present. Also, using the jumpers, select the bipolar output mode for DAC A. When the script is run the ADC will convert the values and debug.exe will display the results. Note that the ADC’s conversions are two’s complement but the DACs’ input is offset binary.

The counter/timer scripts simply put each counter in square-wave mode.

COUNTER_0.DBG	COUNTER_1.DBG	COUNTER_2.DBG
<pre>o 30f 36 o 30c e8 o 30c 03 q</pre>	<pre>o 30f 76 o 30d 64 o 30d 0 q</pre>	<pre>o 30f b4 o 30e ff o 30e 0 q</pre>

The digital I/O scripts will either configure the ports as inputs and read the values at each or configure the ports as outputs and write values to each.

DIO_IN.DBG	DIO_OUT.DBG	DAC_A.DBG
<pre>o 313 9b o 313 1b i 310 i 311 i 312 q</pre>	<pre>o 313 80 o 310 aa o 311 cc o 312 f0 o 313 0 q</pre>	<pre>o 304 ff o 305 3 o 304 ff o 305 7 o 304 ff o 305 b o 304 ff o 305 f o 304 ff o 305 b o 304 ff o 305 7 o 304 ff o 305 3 o 304 0 o 305 0 o 304 ff o 305 3 o 304 ff o 305 7 q</pre>

The DAC script will put a stepped output on pin 2 of connector P3.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesioproducts.com***.. Please detail any errors you find and include your mailing address so that we can send you any manual updates.



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