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MODEL PCIe-DA16-16 High Density Analog Output Multifunction Board USER MANUAL

FILE: PCIe-DA16-16.B4b

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Chapter 1: Introduction

Features

- 16 Channels of Analog Output at 16-bit Resolution
- Available as 12-bit and / or 8-channels
- Software / Hardware compatible with PCI-DA12-16, >125k conversions
- Dip-switch selectable analog output ranges of
  2.5V, 5V, 10V, ±2.5V, ±5V, ±10V, 4-20mA
- Individual or simultaneous update of the DACs
- DACs restricted at power-on to prevent spurious outputs
- 24 Digital I/O Lines
- Four and Eight Bit Ports Independently Selectable for Input or Output
- Pull-Ups on Digital I/O Lines
- Resettable fused VCCIO Supply Available to the User
- Onboard timer can generate interrupts and clock DAC data for waveform generation

Applications

Optical Networking, Instrumentation, Multichannel Data Acquisition and system monitoring, Automatic Test Equipment, Process Control and Industrial Automation, Power line simulation and stimulation. light control, motion control, and more.

Functional Description

Analog Outputs

These cards are 10.5” x 3.875” and can be installed in any PCI Express slot. They contain either eight or sixteen double-buffered digital-to-analog converters (DACs) that provide independent analog output channels of 12- or 16-bit resolution. Each analog output channel can be configured for ranges of:

0V to +2.5V
0V to +5V
0V to +10V
-2.5V to +2.5V
-5V to +5V
-10V to +10V
4mA to 20mA sink

The analog output channels have a double-buffered input for single-step update and each is addressed at its own I/O location. Type DAC80504 quad DAC chips are used. Data is transferred to the FPGA's local registers a byte or word at a time and then

transferred to the DAC buffer registers a word at a time. The analog outputs can then be updated by transferring this data to the DAC active registers either independently, simultaneously by command, or simultaneously by timer.

The DAC outputs are undefined at power-up. Therefore, in order to prevent excessive voltage output to external circuits, the card contains automatic circuits that set D/A outputs to close to 0V at system power-on. Upon power-up, the card is in the Simultaneous Update mode. After all DACs have been loaded with the desired values, a software command can be used to switch the reference voltage to its normal value.

Digital I/O Lines

These cards emulate the 8255 Mode 0 interface providing 24 bits of parallel digital input/output. They can be programmed as inputs or outputs on three 8-bit ports designated Ports A, B, and C. Port C can be further divided into two 4-bit nibbles.

Each I/O line is buffered by a type 74LVC8T245 buffer transceiver capable of sourcing or sinking 32mA (w/ 5V VCCIO), or 24mA (w/ 3.3V VCCIO). Pull-ups on the card assure that there are no erroneous outputs at power up. The lines initialize in the input mode and the I/O line buffers are configured automatically by hardware logic for input or output according to the GROUP Control Register direction software assignment.

Counter Timer

These cards contain FPGA circuitry that emulates a type 8254 counter/timer which has three 16-bit programmable down counters. Counter/Timer #0 is configured for event counting. Counter/Timers #1 and #2 are concatenated and form a 32-bit counter/timer for frequency generation. The dual counter/timer is clocked by a 1 MHZ crystal oscillator and may be gated on/off by a level signal at the connector. The counters can also be programmed to provide a “clock-tick” interrupt and update of the DAC buffers for more precisely timed outputs.

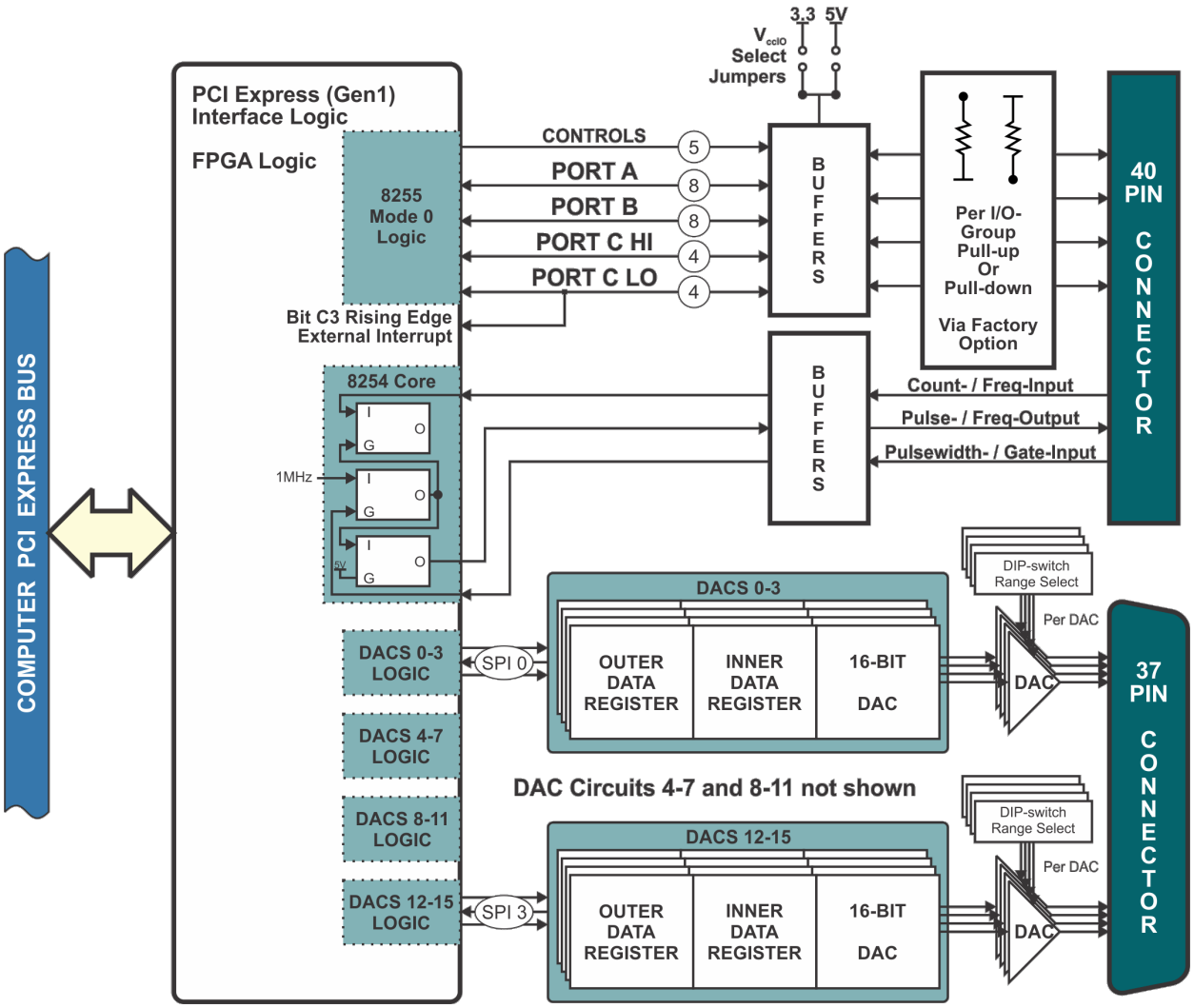


Figure 1-1: Block Diagram

Ordering Guide

PCIe-DA16-16	16-Bit, 16-Channel Analog Output Card
PCIe-DA16-8	16-Bit, 8-Channel Analog Output Card
PCIe-DA12-16	12-Bit, 16-Channel Analog Output Card
PCIe-DA12-8	12-Bit, 8-Channel Analog Output Card

Model Options

-RoHS	RoHS compliant version
-T	Extended operating temperature -40 to +85C

Included with your board

The following components are included with your shipment. Please take time now to ensure that no items are damaged or missing.

PCIe-DA1x-x Board
Adjacent mounting bracket for DB37F connector w/18” ribbon cable for Digital I/O lines

Optional Accessories

ADAP37F-MINI	Direct Plug Spring Cage Terminal Adaptor, use for analog outs
ADAP37M-MINI	Direct Plug Spring Cage Terminal Adaptor use for digital I/O

Chapter 2: Installation

The software provided with this board is available to download via the product page for free and must be installed onto your hard disk prior to use.

Windows

1. Visit the product web page at https://accesio.com/PCIe-DA16-16
2. Download the Software Package from the Manuals / Software tab
3. Run the Install program and follow the on-screen prompts to install the software for this board

Linux

1. Please visit https://github.com/accesio for information on installing under Linux.

Caution! * ESD ***A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.***

Hardware Installation

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETUP.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the computer cover.
5. Carefully install the card in any available PCI Express expansion slot (you may need to remove a backplate first).
6. Inspect for proper fit of the card and tighten the mounting bracket screw. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
7. If you will be using the digital I/O lines on this card, these are accessed using the provided cable assembly with a DB37F connector and mounting bracket. Plug the 40 pin header from this cable assembly onto P3 towards the back end of the card. Then remove an adjacent backplate next to the PCIE-DA card, and install the DB37F mounting bracket from the cable assembly into that backplate slot, install and tighten the mounting bracket screw.
8. Install an I/O cable (or an ADAP37F-MINI) onto the card's bracket mounted male connector.
9. Install an I/O cable (or an ADAP37M-MINI) onto the adjacent mounting bracket with the female connector.
10. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
11. Run AIOWDMFind.exe to complete installing the card into the registry (for Windows only) and to determine the assigned resources.
12. Run one of the provided sample programs that was copied to the newly created card directory to test and validate your installation.

The base address assigned by BIOS or the operating system can change each time new hardware is installed into or removed from the computer. Please recheck AIOWDMFind.exe or Device Manager if the hardware configuration is changed. Software you write can automatically determine the base address of the card using a variety of methods depending on the operating system. In Windows, the Windows sample programs demonstrate querying the registry entries (created by AIOWDMFind and NTIOPCI.SYS during boot-up) to determine this same information.

Chapter 3: Option Selection

Voltage output ranges are determined by switch settings as described in the following paragraphs. Also, the method to update D/A outputs is programmable as described here and in Chapter 5, Programming.

Output Ranges

There is a four-position slide switch (OFF = DOWN position / ON = UP position) with each individual position slide notated with 1, 2, 3 or 4. Each four-position slide switch is associated with each DAC channel to make voltage range selection: switches S1 (Channel 0) through S16 (Channel 15) as depicted in the following table.

Voltage Range	**1**	**2**	**3**	4
0 to +2.5V	OFF	ON	ON	OFF
0 to +5V	OFF	OFF	OFF	OFF
0 to +10V	OFF	OFF	ON	OFF
-2.5V to +2.5V	ON	ON	ON	OFF
-5V to +5V	ON	OFF	OFF	OFF
-10V to +10V	ON	OFF	ON	OFF
4 mA to 20 mA	OFF	OFF	OFF	ON

Analog Output Update

Analog outputs are updated under program control in any of two ways:

a. Automatic Update: Each channel is updated individually when new data are written to the related high-byte base address. Individual update mode may be set by a special read operation as defined in the programming section of this manual.

b. Simultaneous Update: The outputs of all D/As may be updated simultaneously. This is done by first enabling simultaneous updating for all outputs, preloading the low and high bytes of each DAC, and then initiating a simultaneous update by software command or waveform timer tick.

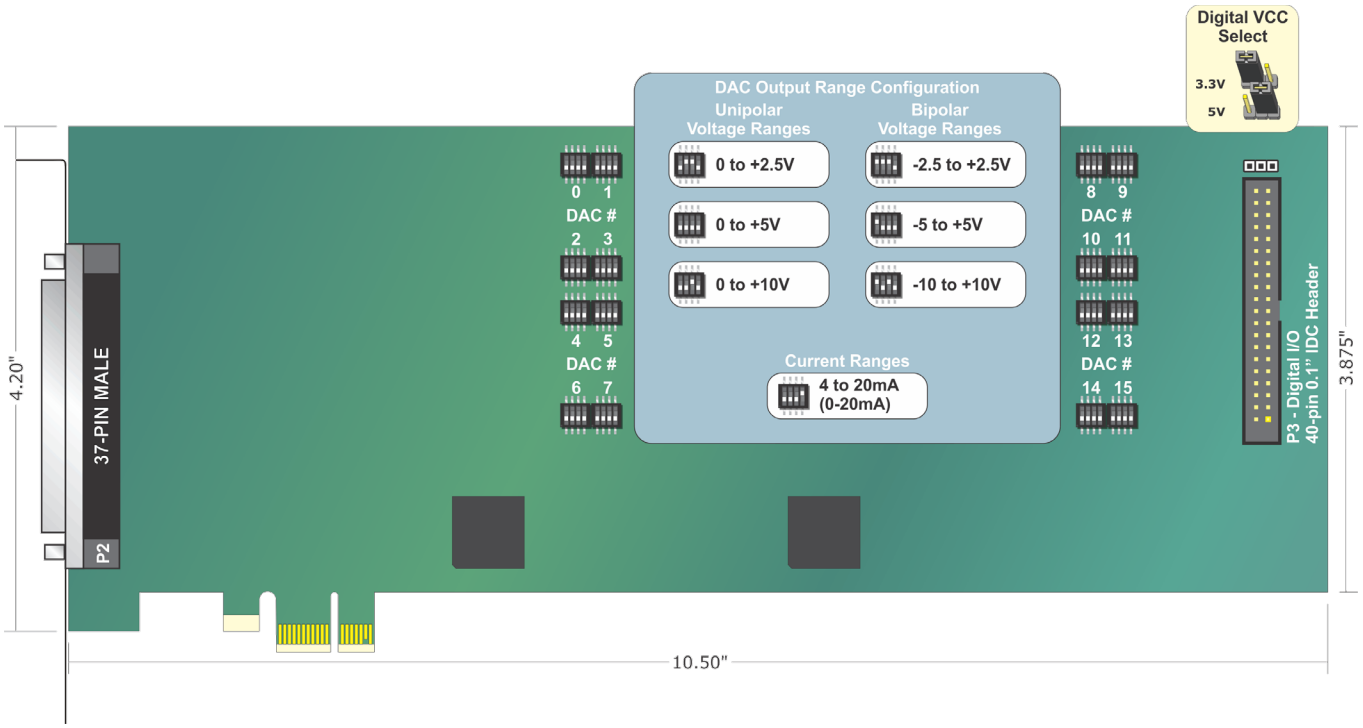


Figure 3-1: Option Selection Map

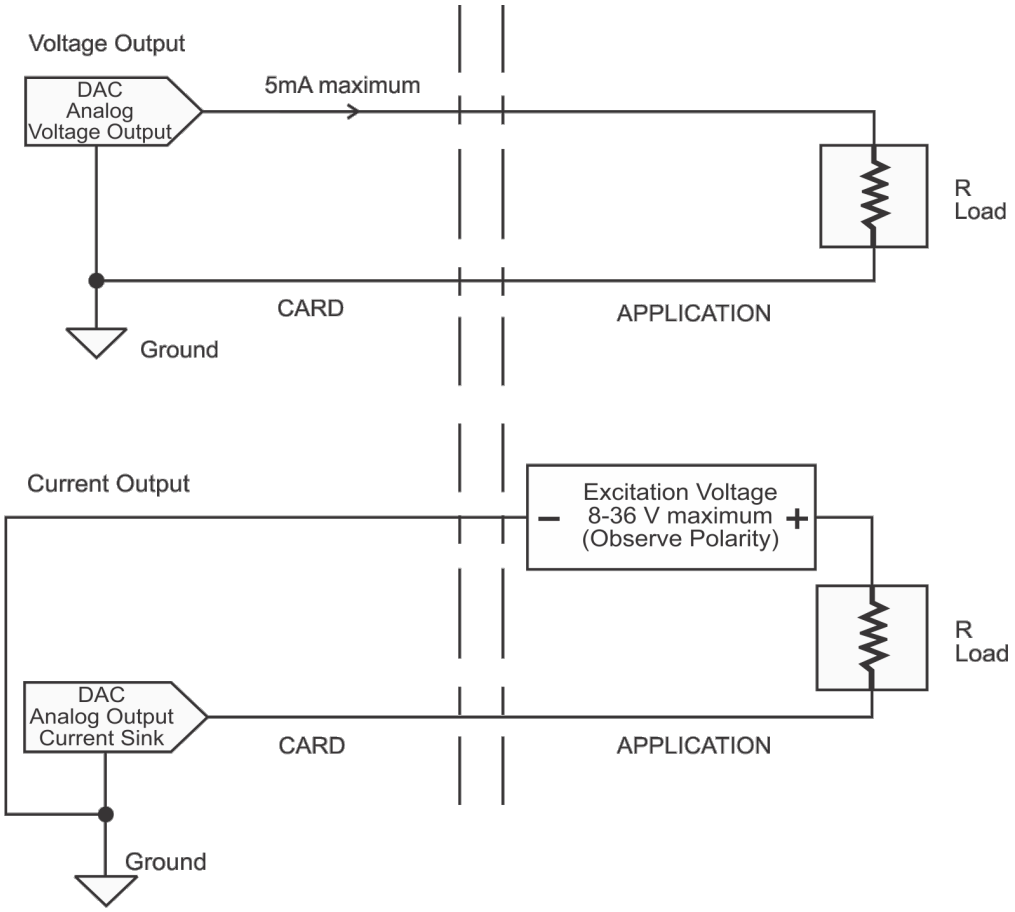


Figure 3-2: Field Wiring Diagrams

Caution!
Do not connect current loops in a DAC that is set to voltage mode. The loop supply can destroy the DAC.

Chapter 4: Address Selection

These cards use three address spaces. These are defined in the Port Address Selection Table in the Programming section of this manual.

PCI Express architecture is inherently plug-and-play. This means that the BIOS or Operating System determines the resources assigned to PCI Express cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the AIOWDMFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI Express bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, some operating systems can be queried to determine which resources were assigned. In these operating systems, you can use either AIOWDMFind (Windows 7 or later) PCIFind or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for these cards is 494F. (ASCII for "IO")

The Device ID for the 16-bit 16 channel card is 48f0h.
The Device ID for the 16-bit 8 channel card is 48e8h.
The Device ID for the 12-bit 16 channel card is 48b0h.
The Device ID for the 12-bit 8 channel card is 48a8h.

Chapter 5: Programming

The cards' DACs, Timers, and Digital I/O use 40 consecutive I/O addresses. Programming these cards is very straightforward as there are only three operating modes and four range-selection switches per channel. The basic operation of a Digital-to-Analog card is to write a 16-bit value to a Digital to Analog Converter (DAC) where it is buffered and loaded by an update command to a DAC active register. Outputs of that register control a "ladder" network which produces the analog output. The output voltage range is defined by settings of the range-selection switches for that channel. For example:

```
double spanVolts = 10.0;  // for ±5V; use "20.0" for ±10
double offsetVolts = spanVolts / 2; //use "0.0" for all unipolar ranges.
double targetVolts = 1.3; // change to any desired output voltage
counts = (targetVolts + offsetVolts) / spanVolts * 65536.0;
RelOutPort(DeviceIndex, DAC * 2, counts);
```

Upon power-up, or hardware reset, the DAC registers are restricted to a safe value and the card is set in Simultaneous Update mode. Since the pre-load register is not cleared upon power-up, but left at an undefined value, a known value must be written to the preload registers before using a "Clear Restrict-Output-Voltage" command.

Simultaneous Update Mode is the power-up or default mode of operation for the DAC card. When a value is written to a DAC address the output does not change until an output update is commanded via a read from Base Address+8. (Alternatively, a read of Base Address+A will update the DAC registers and switch the board to Automatic Update Mode.) While in Simultaneous Update Mode, a single read will load all DAC registers with the value waiting in the pre-load registers, causing all outputs to be updated and changed simultaneously.

Automatic Update Mode is the configuration that changes a DAC output immediately after the high-byte of the new value is written to the DAC address. If the card is in Simultaneous Update Mode a read of Base Address+2 will change the card back to Automatic Update Mode without updating the outputs. A read of Base Address+A will update all outputs simultaneously and then place the card in Automatic Update Mode.

Timer Update Mode is similar to Simultaneous Update Mode, except that updates are issued by the counter/timer (programmed in mode 2 or mode 4 per Chapter 6, Programming 8254). A read from Base Address+5 will change the card from Simultaneous Update Mode to Timer Update Mode, and a read from Base Address+6 will change it back. The counter-generated update pulse is also available at the 40-pin header connector(OUT2) to synchronize external devices, and can generate interrupts for synchronized loading if enabled by a read from Base Address+3. (Interrupts are disabled by a read from Base Address+4.)

Restrict-Output-Voltage limits the output of all DAC channels to 0V and is active at power-up. Since the pre-load register defaults to its min-scale value, known values can be written to the preload registers before using a "Clear Restrict-Output-Voltage" command. Those written values will then be output to the connector when a "Clear Restrict-Output-Voltage" command is issued by a read of Base Address +F.

Address	Write *	Read
Base + 0	DAC 0 Low Byte	Place card in Simultaneous Mode without updating outputs.
Base + 1	DAC 0 High Byte	
Base + 2	DAC 1 Low Byte	Release card from Simultaneous Mode without updating outputs.
Base + 3	DAC 1 High Byte	Enable Interrupts
Base + 4	DAC 2 Low Byte	Disable Interrupts
Base + 5	DAC 2 High Byte	Enable Timer Initiated DAC Update
Base + 6	DAC 3 Low Byte	Disable Timer Initiated DAC Update
Base + 7	DAC 3 High Byte	
Base + 8	DAC 4 Low Byte	Update all outputs and place card in Simultaneous Mode.
Base + 9	DAC 4 High Byte	
Base + A	DAC 5 Low Byte	Update all outputs and release card from Simultaneous Mode.
Base + B	DAC 5 High Byte	
Base + C	DAC 6 Low Byte	Clear IRQ
Base + D	DAC 6 High Byte	
Base + E	DAC 7 Low Byte	Restrict-Output-Voltage (Disables voltage reference)
Base + F	DAC 7 High Byte	Clear Restrict-Output-Voltage (Allows full operating output voltage).
Base + 10	DAC 8 Low Byte	
Base + 11	DAC 8 High Byte	
Base + 12	DAC 9 Low Byte	
Base + 13	DAC 9 High Byte	
Base + 14	DAC 10 Low Byte	
Base + 15	DAC 10 High Byte	
Base + 16	DAC 11 Low Byte	
Base + 17	DAC 11 High Byte	
Base + 18	DAC 12 Low Byte	
Base + 19	DAC 12 High Byte	
Base + 1A	DAC 13 Low Byte	
Base + 1B	DAC 13 High Byte	
Base + 1C	DAC 14 Low Byte	
Base + 1D	DAC 14 High Byte	
Base + 1E	DAC 15 Low Byte	
Base + 1F	DAC 15 High Byte	
Base + 20	Digital I/O Port A, Output	Digital I/O Port A, Input
Base + 21	Digital I/O Port B, Output	Digital I/O Port B, Input
Base + 22	Digital I/O Port C, Output	Digital I/O Port C, Input
Base + 23	Digital I/O Control Byte	
Base + 24	Counter/Timer 0	Counter/Timer 0
Base + 25	Counter/Timer 1	Counter/Timer 1
Base + 26	Counter/Timer 2	Counter/Timer 2
Base + 27	Counter/Timer Control Register	Counter/Timer Control Register

Table 5-1: Register Map

Restrict-Output-Voltage limits the output of all DAC channels and is active at power-up.

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Low Byte	B7	B6	B5	B4	B3	B2	B1	B0
High Byte	*B15	*B14	*B13	*B12	B11	B10	B9	B8

Table 5-2: DAC Data Format

* B15->B12 are ignored by 12-bit models

For Unipolar ranges, data is in true binary form.

```
                0000  0000  0000  0000    =  Zero (Low Scale)
                1000  0000  0000  0000    =  ½ Scale
                1111  1111  1111  1111    =  Full Scale
                |                   |
MSB or B15      ←                   →       B0 or LSB
```

For Bipolar ranges, data are in offset binary form. (Same as above)

Programming the Digital I/O Circuit

The digital I/O circuit is comprised of an emulated 8255, a direction control latch, and four bi-directional buffers with 10K pull-ups.

The cards are designed to emulate each GROUP wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.
e. The card is initialized in the input mode

Each GROUP contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each GROUP should be configured during initialization by writing to the control registers even if the ports are going to be used as inputs. Output buffers are automatically set by hardware logic according to the control register states. Control registers are located at base address +23. Bit assignments in each of these control registers are as follows:

Bit	Assignment	Function
D0	Port C Lo (C0-C3)	1 = Input, 0 = Output
D1	Port B	1 = Input, 0 = Output
D2	N/A	N/A
D3	Port C Hi (C4-C7)	1 = Input, 0 = Output
D4	Port A	1 = Input, 0 = Output
D5,D6	N/A	N/A
D7	Mode Set (see note 1)	Scratchpad

Table 5-3: Control Register Bit Assignments

Note 1: This bit is a read/write scratchpad. For maximum compatibility with the 8255, always set this bit (to 1).

Chapter 6: Timer-Driven DAC “waveform” update mode

The onboard counter/timer can be used to initiate simultaneous DAC updates on each timer tick, allowing hardware-timed waveform generation. Each timer tick can also fire an IRQ, informing your application it needs to update the DAC Load registers with the next point of waveform data.

To set the Timer Driven DAC Waveform Update / IRQ Rate you program the onboard (emulated) concatenated counters 1+2 for Mode 2 then load the number of microseconds between ticks (divided into the two 16-bit counters).

Read from Base + 0 to put the card in Simultaneous Update mode:
```
RelInPortB(CardNum, 0)l
```

Write 0b01111000 to the control register at Base + 27 to set CTR1 to Mode 2:
```
RelOutportB(CardNum, 0x27, 0x78);
```

Write 0b10111000 to the control register at Base + 27 to set CTR2 to Mode 2:
```
RelOutportB(CardNum, 0x27, 0xB8);
```

Calculate the divisor for the target rate and split it into the two counters' (re-)load registers:

TargetUpdateRateHz = 1000
BaseCounterRateHz = 1000000
FullDivisor = BaseCounterRateHz ÷ TargetUpdateRateHz:
FullDivisor = 1000
CTR1Divisor = FullDivisor ÷ 2*: CTR1Divisor = 500
CTR2Divisor = FullDivisor ÷ CTR1Divisor: CTR2Divisor = 2

Write LSB(CTR1Divisor) to the control register at Base + 25:
```
RelOutportB(CardNum, 0x25, LSB(500));
```

Write MSB(CTR1Divisor) to the control register at Base + 25:
```
RelOutportB(CardNum, 0x25, MSB(500));
```

Write LSB(CTR2Divisor) to the control register at Base + 26:
```
RelOutportB(CardNum, 0x26, LSB(2));
```

Write MSB(CTR2Divisor) to the control register at Base + 26:
```
RelOutportB(CardNum, 0x26, MSB(2));
```

This will cause the CTR2 output to "tick" at 1000Hz.

To enable the tick to load the DACs write read from Base + 0x05:
```
RelInportB(CardNum, 0x05);
```

To enable the tick to generate an IRQ read from Base + 0x03:
```
RelInportB(CardNum, 0x03);
```

To clear the IRQ latch read from Base + 0x0c:
```
RelInportB(CardNum, 0x0c); // this is normally handled by the AIOWDM
driver in Windows
```

Each IRQ you just have to load the DACs with the next data point to be output and it will occur on the next timer tick automatically.

Chapter 7: Software

These cards are straightforward to program. The following example is in C, but sample code is also provided on the CD in Pascal and four Windows languages: Delphi, VisualBASIC, and Visual C++.

To output an analog value with 16-bit resolution, a corresponding decimal number N between 0 and 65535 is calculated (2^{16} = 65536).

```
counts = (targetVolts + offsetVolts) / spanVolts * 65536.0;
```

Next the data are written to the selected analog output channel. (See the preceding I/O Address Map.) In this example, we will assume analog output on channel zero (AO 0).

```
RelOutport(DeviceIndex, 0, counts);
```

For simplicity, it was assumed that the simultaneous-update capability was not used.

Examples of this routine are installed with the software package along with examples in other languages.

Chapter 8: Calibration

Periodic calibration of these cards is recommended if they are used in extreme environmental conditions. The card uses very stable components but high-low temperature cycles might result in slight analog output errors.

The following equation is used with 16-bit cards:

```
Calibrated = ((4096 – LowAdjust - HighAdjust) / 4096) * Counts + 16 * LowAdjust
```

The 12-bit card is calibrated by software using the following formula:

```
Calibrated = ((4096 – LowAdjust - HighAdjust) / 4096) * Counts + LowAdjust
```

To calibrate the card, run the calibration program and follow the screen prompts. No attempt at calibration should be made in noisy locations or with a noisy calibration setup.

The calibration program stores various data to the card to facilitate calibrating the data output in a run-time environment. The data collected during calibration is stored in an EEPROM located at the second of the I/O base addresses assigned to the device (BaseAddresses[3] in the PCI_COMMON_CONFIG structure). The EEPROM contains two values per channel per range. The ZERO (or LowAdjust) and the HighAdjust calibration constants are stored (a and b from the equation above) for each channel at each possible range (0-6). These constants are used during normal operation to calibrate the output data in real-time. Refer to the samples provided on disk for an example of using this data.

EEPROM Offset (hex)	Range	DAC	Calibration Constant
+00	0-5V	DAC 0	LowAdjust
+01	0-5V	DAC 0	HighAdjust
+02..3	0-5V	DAC 1	LowAdjust, HighAdjust
+04..1D	0-5V	DAC 3..14	LowAdjust, HighAdjust
+1E..1F	0-5V	DAC 15	LowAdjust, HighAdjust
+20..3F	0-2.5V	DAC 0..15	LowAdjust, HighAdjust
+40..5F	0-10V	DAC 0..15	LowAdjust, HighAdjust
+60..7F	±5V	DAC 0..15	LowAdjust, HighAdjust
+80..9F	±2.5V	DAC 0..15	LowAdjust, HighAdjust
+A0..BF	±10V	DAC 0..15	LowAdjust, HighAdjust
+C0..DF	4-20mA	DAC 0..15	LowAdjust, HighAdjust

The current Range Code configured at the per-channel range switches can be read from the BAR[3] “CalBase” registers, starting at +F0.

The value stored is a number from 0 to 6, representing the 7 ranges (as shown in the table below). These are read from the range selection switches in real time.

Word Address	Channel
Base + F0h	Channel 0
Base + F1h	Channel 1
Base + F2h	Channel 2
Base + F3h	Channel 3
Base + F4h	Channel 4
Base + F5h	Channel 5
Base + F6h	Channel 6
Base + F7h	Channel 7
Base + F8h	Channel 8
Base + F9h	Channel 9
Base + FAh	Channel 10
Base + FBh	Channel 11
Base + FCh	Channel 12
Base + FDh	Channel 13
Base + FEh	Channel 14
Base + FFh	Channel 15

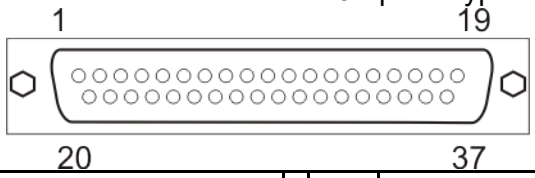
Value	Range
0	0 - 5 V
1	0 - 2.5 V
2	0 - 10 V
3	-5 - +5 V
4	-2.5 - +2.5V
5	-10 V - +10 V
6	4-20mA

The currently configured Range Code for each DAC can be read using the following code:

```
RangeCode = inportb(CalBase + 0xF0 + DAC);
```

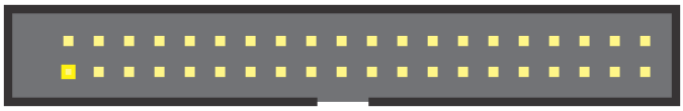
Chapter 9: Connector Pin Assignments

The analog outputs are accessible via a male 37-pin D type connector.



Pin	Name	Function		Pin	Name	Function
1	D/A 0 Out	Analog DAC 0 Output		20	Analog GND	Analog Ground
2	D/A 1 Out	Analog DAC 1 Output		21	Analog GND	Analog Ground
3	D/A 2 Out	Analog DAC 2 Output		22	Analog GND	Analog Ground
4	D/A 3 Out	Analog DAC 3 Output		23	Analog GND	Analog Ground
5	D/A 4 Out	Analog DAC 4 Output		24	Analog GND	Analog Ground
6	D/A 5 Out	Analog DAC 5 Output		25	Analog GND	Analog Ground
7	D/A 6 Out	Analog DAC 6 Output		26	Analog GND	Analog Ground
8	D/A 7 Out	Analog DAC 7 Output		27	Analog GND	Analog Ground
9	D/A 8 Out	Analog DAC 8 Output		28	Analog GND	Analog Ground
10	D/A 9 Out	Analog DAC 9 Output		29	Analog GND	Analog Ground
11	D/A 10 Out	Analog DAC 10 Output		30	Analog GND	Analog Ground
12	D/A 11 Out	Analog DAC 11 Output		31	Analog GND	Analog Ground
13	D/A 12 Out	Analog DAC 12 Output		32	Analog GND	Analog Ground
14	D/A 13 Out	Analog DAC 13 Output		33	Analog GND	Analog Ground
15	D/A 14 Out	Analog DAC 14 Output		34	Analog GND	Analog Ground
16	D/A 15 Out	Analog DAC 15 Output		35	Analog GND	Analog Ground
17	N/C	No Connection		36	VCCIO Vout	Fused VCCIO Output
18	Analog GND	Analog Ground		37	Digital GND	Digital Ground
19	Analog GND	Analog Ground				

Table 9-1: P2 DAC Pin Assignments DB37M



The digital I/O and counter outputs are accessible on the board via a 40-pin IDC header. A ribbon cable assembly with a 40-pin header and a DB37 female connector with a mounting bracket is shipped with the card.

Pin	Function	Pin	Function
1	Digital I/O Port A - Bit 0	21	Digital I/O Port C - Bit 0
2	Digital I/O Port A - Bit 1	22	Digital I/O Port C - Bit 1
3	Digital I/O Port A - Bit 2	23	Digital I/O Port C - Bit 2
4	Digital I/O Port A - Bit 3	24	Digital I/O Port C - Bit 3
5	Digital I/O Port A - Bit 4	25	Digital Ground
6	Digital I/O Port A - Bit 5	26	Digital Ground
7	Digital I/O Port A - Bit 6	27	Digital I/O Port C - Bit 4
8	Digital I/O Port A - Bit 7	28	Digital I/O Port C - Bit 5
9	Digital Ground	29	Digital I/O Port C - Bit 6
10	Digital Ground	30	Digital I/O Port C - Bit 7
11	Digital I/O Port B - Bit 0	31	Digital Ground
12	Digital I/O Port B - Bit 1	32	Digital Ground
13	Digital I/O Port B - Bit 2	33	Clock In
14	Digital I/O Port B - Bit 3	34	Gate
15	Digital I/O Port B - Bit 4	35	Clock Out
16	Digital I/O Port B - Bit 5	36	Digital Ground
17	Digital I/O Port B - Bit 6	37	Digital Ground
18	Digital I/O Port B - Bit 7	38	Digital Ground
19	Digital Ground	39	Digital Ground
20	Digital Ground	40	Digital Ground

Table 9-2: P3 Digital I/O & Counter/Timer Pin Assignments

Pin	Function	Pin	Function
1	Digital I/O Port A - Bit 0	20	Digital I/O Port A - Bit 1
2	Digital I/O Port A - Bit 2	21	Digital I/O Port A - Bit 3
3	Digital I/O Port A - Bit 4	22	Digital I/O Port A - Bit 5
4	Digital I/O Port A - Bit 6	23	Digital I/O Port A - Bit 7
5	Digital Ground	24	Digital Ground
6	Digital I/O Port B - Bit 0	25	Digital I/O Port B - Bit 1
7	Digital I/O Port B - Bit 2	26	Digital I/O Port B - Bit 3
8	Digital I/O Port B - Bit 4	27	Digital I/O Port B - Bit 5
9	Digital I/O Port B - Bit 6	28	Digital I/O Port B - Bit 7
10	Digital Ground	29	Digital Ground
11	Digital I/O Port C - Bit 0	30	Digital I/O Port C - Bit 1
12	Digital I/O Port C - Bit 2	31	Digital I/O Port C - Bit 3
13	Digital Ground	32	Digital Ground
14	Digital I/O Port C - Bit 4	33	Digital I/O Port C - Bit 5
15	Digital I/O Port C - Bit 6	34	Digital I/O Port C - Bit 7
16	Digital Ground	35	Digital Ground
17	Clock In	36	Gate
18	Clock Out	37	Digital Ground
19	Digital Ground		

Table 9-3: Digital I/O & Counter/Timer Pin Assignments, DB37F

Chapter 10 Specifications

Analog Outputs

- Channels: 16, 8
- Resolution: 16 bits, 12 bits
- Unipolar Ranges: 0-2.5V, 0-5V, 0-10V
- Bipolar Ranges: ±2.5V, ±5.0V, ±10.0V
- Current Range: 4 to 20 mA (external excitation of 8-36VDC)
- Output Drive: 5 mA maximum
- Output Resistance: Less than 0.1 ohm
- Relative Accuracy: ± 1 LSB max, ± ½ LSB typical
- Diff. Linearity: ± ½ LSB integral non-linearity
- Monotonicity: 16 bits over operating temp
- Settle time: 5 µsec ¼ to ¾ and ¾ to ¼ scale, to ±2 LSB

Digital I/O

- Lines 24: Ports A, B, and C
- Type 8255 compatible
- Logic Level: VCCIO jumper selectable
- Pull-up/down 10k ohm (pulled up by default)

Logic Levels	**VCCIO = 5V**	
Low Inputs	≤ 1.5V	≤ 2uA
High Inputs	≥ 3.5V	≤ 2uA
Low Outputs	≤ 0.55V	32mA
High Outputs	≥ 3.8V	32mA
Logic Levels	**VCCIO = 3.3V**	
Low Inputs	≤ 0.8V	≤ 2uA
High Inputs	≥ 2.0V	≤ 2uA
Low Outputs	≤ 0.55V	24mA
High Outputs	≥ 2.4V	24mA

Counter/Timer

- Type: Emulated 8254 programmable counters
- Counter size: 16-bit
- Logic level: VCCIO
- On-board clock 1MHz

Environmental

- Operating Temp: 0 to +70°C
- Storage Temp: -55 to +150°C
- Humidity: 5% to 95% w/o condensation
- PCIe-DA16-8/16: 10.5" (267 mm) long

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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